REMARKS/ARGUMENTS

Brief Summary of Status

Claims 1-184 are pending in the application.

Claims 1-184 are rejected.

Double Patenting

1. In the office action, the Examiner states:

"Applicant is advised that should claim 175 be found allowable, claims 176, 179, and 181 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. Applicant is advised that should claim 178 be found allowable, claims 177, 180, and 182 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k)." (office action, Part of Paper No./Mail Date Part of Paper No./Mail Date 20050929, p. 2).

Claim Rejections - 35 U.S.C. § 102

2. In the office action, the Examiner states:

"Claims 1-29, 34-71, 76-79, 113-116, 119-128, 134-162, 167-174, 179, and 180 are rejected under 35 U.S.C. 102(e) as being anticipated by Phanse (US 6,795,494)." (hereinafter referred to as "PHANSE") (office action, Part of Paper No./Mail Date 20050929, p. 2).

Claim Rejections - 35 U.S.C. § 103

3. In the office action, the Examiner states:

"Claims 30 - 33, 72 - 75, 80 - 112, 117, 118, and 163 - 166 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phanse('494) in view of Jamali (US-6,678,319)." (Jamali (US-6,678,319) is hereinafter referred to as "JAMALI") (office action, Part of Paper No./Mail Date 20050929, p. 9).

4. In the office action, the Examiner states:

"Claims 129 - 133, 175 - 178, and 181 - 184 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phanse ('494) in view of Apple (US-5,239,299)." (Apple (US-

5,239,299)" is hereinafter referred to as "APPLE") (office action, Part of Paper No./Mail Date 20050929, p. 11).

Double Patenting

1. In the office action, the Examiner states:

"Applicant is advised that should claim 175 be found allowable, claims 176, 179, and 181 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. Applicant is advised that should claim 178 be found allowable, claims 177, 180, and 182 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k)." (office action, Part of Paper No./Mail Date Part of Paper No./Mail Date 20050929, p. 2).

The Applicant provided a portion from MPEP § 706.03(k) below:

"Inasmuch as a patent is supposed to be limited to only one invention or, at most, several closely related indivisible inventions, limiting an application to a single claim, or a single claim to each of the related inventions might appear to be logical as well as convenient. However, court decisions have confirmed applicant's right to restate (i.e., by plural claiming) the invention in a reasonable number of ways. Indeed, a mere difference in scope between claims has been held to be enough.

Nevertheless, when two claims in an application are duplicates, or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other claim under 37 CFR 1.75 as being a substantial duplicate of the allowed claim." (MPEP § 706.03(k), 700-74 to 700-75, Rev. 3, August 2005).

The Applicant respectfully points out some distinctions between some of the Examiner identified claims to support the Applicant's belief that they do not "duplicates" of one another, and that that they do not "cover the same thing".

When comparing independent claims 175 and 176, the Applicant respectfully asserts that, at a very minimum, independent claim 176 includes the limitation of the digital signal processor demodulates the digital samples using parallel processing techniques to extract the digital data contained therein, whereas independent claim 175 does not.

Given that Examiners are to provide the broadest reasonable interpretation of the claims that is consistent with the specification (e.g., as described at least in MPEP § 2111, 2100-46 to 2100-47, Rev. 3, August 2005), the Applicant respectfully believes that claim 175 should well be interpreted to include subject matter such that the digital signal processor demodulates the digital samples using processing techniques other than parallel to extract the digital data contained therein.

Moreover, when comparing various claims, the Applicant respectfully asserts that "[o]ffice personnel should begin claim analysis by identifying and evaluating each claim limitation." (MPEP § 2111, 2100-8, Rev. 3, August 2005, emphasis added).

Independent claim 175 includes the at least the subject matter of a transceiver, comprising: a serializer/de-serializer receiver, that receives modulated serial data from a serializer/de-serializer transmitter, that includes a plurality of interleaved analog to digital converters and a digital signal processor, the digital signal processor being communicatively coupled to an output of the plurality of interleaved analog to digital converters; the plurality of interleaved analog to digital converters operate cooperatively to sample the modulated serial data to generate digital samples of the modulated serial data; and the digital signal processor demodulates the digital samples to extract the digital data contained therein.

Independent claim 179 includes at least the subject matter of a transceiver, comprising: a serializer/de-serializer receiver, that receives the modulated serial data from a serializer/de-serializer transmitter, that includes an analog to digital converter and a digital signal processor, the digital signal processor being communicatively coupled to an output of the analog to digital converter; the analog to digital converter samples modulated serial data to generate digital samples of the modulated serial data; and the digital signal processor demodulates the digital samples using parallel processing techniques to extract the digital data contained therein.

When comparing independent claims 175 and 179, the Applicant respectfully points out that independent claim 179 does not include any reference to a plurality of interleaved analog to digital converters. The analog to digital converter of independent claim 179 need not necessarily be within a plurality of analog to digital converters (i.e., independent claim 179 does not even include the limitation "plurality" therein), and the

analog to digital converter need not necessarily be within a plurality of interleaved analog to digital converters.

As such, the Applicant respectfully believes that the independent claims 175 and 179 do in fact distinctly claim different subject matter, and the Applicant respectfully believes that these claims do not "both cover the same thing". For example, looking at these examples, the claimed subject matter of claim 175 describes a plurality of interleaved analog to digital converters, whereas the subject matter of claim 179 describes an analog to digital converter.

Comparisons can be made when comparing the other claims identified above with respect to the differentiations of subject matter that each one claims.

As such, the Applicant respectfully requests that the Examiner identify and evaluate each claim limitations with respect to the independent claims 175-182.

Claim Rejections - 35 U.S.C. § 102

2. In the office action, the Examiner states:

"Claims 1-29, 34-71, 76-79, 113-116, 119-128, 134-162, 167-174, 179, and 180 are rejected under 35 U.S.C. 102(e) as being anticipated by Phanse (US 6,795,494)." (hereinafter referred to as "PHANSE") (office action, Part of Paper No./Mail Date 20050929, p. 2).

The Applicant respectfully traverses.

The Applicant respectfully submits that if a reference, as considered individually as required under 35 U.S.C. §102, fails to disclose each and every element of the subject matter as claimed by the Applicant, then the rejection under 35 U.S.C. §102 should be withdrawn.

In the above referenced office action, the Examiner asserts:

"With regard to claim 1, Phanse discloses a DSP based serializer 1 de-serializer (see abstract) comprising: a receiver that includes an AID converter and a DSP, the DSP is operably coupled to the output of the AID converter (see figure 1, 145, 150, 180 and abstract); wherein AID converter samples modulated serial data to generate digital samples of modulated serial data (see figure 1, 145 and abstract); and the DSP adaptively determines compensation operations to be performed by the receiver on digital samples

of modulated serial data so that digital samples of modulated serial data may be properly characterized to extract digital data contained therein (see abstract)." (office action, Part of Paper No./Mail Date 20050929, p. 2)

The Applicant respectfully points out that FIG. 1 of PHANSE does not include any digital signal processor.

The first mention in PHANSE of anything like a digital signal processor is with reference to FIG. 7 and is cited as follows:

PHANSE discloses:

"The digital back-end of full-duplex transceiver 700 comprises digital FIR filter 150, digital signal processor (DSP) echo canceller and near-end crosstalk (NEXT) canceller 710, DSP automatic gain control (AGC) circuit 720, DSP base line wander (BLW) circuit 730, DSP adaptive controller 740, and slicer 155. Digital FIR filter 150 and slicer 155 are the same as in full-duplex transceiver 100. However, digital FIR controller 180 has been replaced by DSP adaptive controller 740, which not only generates coefficients for digital FIR filter 150, but also controls the operations of DSP echo canceller and NEXT canceller 710, DSP AGC circuit 720, and DSP BLW circuit 730." (PHANSE, col. 11, lines 27-38, emphasis added)

In performing the "digital signal processing" capabilities within FIG. 7 of PHANSE, PHANSE employs at least 4 separate devices:

1. digital signal processor (DSP) echo canceller and near-end crosstalk (NEXT) canceller 710;
2. DSP automatic gain control (AGC) circuit 720;
3. DSP base line wander (BLW) circuit 730; and
4. DSP adaptive controller 740.

As the Applicant describes in more detail below, FIG. 7 operates using digital domain compensation in conjunction with analog domain based compensation.

Referring back to FIG. 1 of PHANSE, which the Examiner references, the Applicant also respectfully points out that FIG. 1 of PHANSE depicts at least 3 separate functional blocks (SLICER 135, DIGITAL FIR FILTER 150 and DIGITAL FIR CONTROLLER 180) that operate cooperatively to process the output of the ADC 145. The Applicant respectfully asserts that the DIGITAL FIR FILTER 150 of PHANSE is a

passive type device that seems to be governed and operated totally by the DIGITAL FIR CONTROLLER 180 as depicted in FIG. 1 of PHANSE.

The ABSTRACT of PHANSE discloses:

"There is disclosed a transceiver for use in a high speed Ethernet local area network (LAN). The transceiver comprises: 1) front-end analog signal processing circuitry comprising: a) a line driver for transmitting an outgoing analog signal to an external cable; b) a DC offset correction circuit for reducing a DC component in an incoming analog signal; c) an echo canceller; d) an automatic gain control (AGC) circuit; and e) an adaptive analog equalization filter. The transceiver also comprises: 2) an analog-to-digital converter (ADC) for converting the analog filter incoming signal to a first incoming digital signal; and 3) digital signal processing circuitry comprising: a) a digital finite impulse response (FIR) filter; b) a digital echo cancellation circuit to produce a reduced-echo incoming digital signal; c) a digital automatic gain control (AGC) circuit; and d) a digital base line wander circuit." (PHANSE, Abstract)

PHANSE also discloses:

"Analog-to-digital converter (ADC) 145 converts the filtered analog data signals from AEF 140 to digital signals. The digital output signals from ADC 145 are then transferred to digital finite impulse response (FIR) filter 150 and to data slicer 155. The filter tap coefficients of digital FIR filter 150 are used to adjust the equalization of AEF 140. Slicer 155 detects the five levels of the PAM-5 signal and generates both an output data signal and an output error signal. Slicer 155 determines the error between the signal levels of the data symbols generated by digital FIR filter 150 and the ideal signal levels of the modulation technique. For example, in a five-level pulse amplitude modulation (PAM-5) system, data is represented by five voltage levels, designated as an alphabet symbol having values of -2, -1, 0, +1, +2 volts. If slicer 155 receives a voltage level of, for example, +1.15 volts, slicer 155 determines that the received signal level was supposed to be +1.0 volts and cuts off the +0.15 volt error signal. The slicer error signals are used to control the amount of echo cancellation and to determine the values of the filter tap coefficients used by digital FIR filter 150.

During normal operation, AGC 135 and AGC controller 170 amplify the incoming signal to a level that is sufficiently below the maximum limits of ADC 145

such that the expected maximum signal peaks of the incoming signal are not large enough to saturate ADC 145. However, in some embodiments, the signal levels of the output of ADC 145 may not match the signal levels expected by slicer 155. That is, it may not be possible to operate ADC 145 to reach the signal levels suitable for slicer 155 without sacrificing the extra headroom needed to prevent saturation of ADC 145. To compensate for this, in an advantageous embodiment of the present invention, digital FIR filter 150 may also apply a flat gain to the digital output of ADC 145 in addition to applying signal equalization to the output of ADC 145. The gain applied by digital FIR filter 150 may scale up or scale down the digital output signals from ADC 145." (PHANSE, col. 6, line 37 to col. 7, line 7, emphasis added)

The signals that are output from the ADC 145 of PHANSE must be processed by at least 3 separate functional blocks that all operate in conjunction with one another to perform any digital based compensation on the output of the ADC 145, and the system of FIG. 1 of PHANSE also performs analog domain based compensation in conjunction with this digital domain based compensation, in that, the digital domain compensation seems incapable to perform without the analog domain based compensation.

Furthermore, the Applicant respectfully points out that the compensation performed by these functional blocks within the "digital back-end processing components" is not limited to the digital circuitry portions therein, these digital domain components operate in conjunction with the analog components in the analog front end portion.

Moreover, in FIG. 1 of PHANSE, the Applicant respectfully points out that the output of the ADC 145 is modified in the digital domain by digital FIR filter 150. The Applicant respectfully asserts that the digital FIR filter 150 is a passive type device whose operation is governed solely by the digital filter controller 180.

PHANSE discloses:

"The operation of digital FIR filter 150 is controlled by digital FIR filter controller 180." (PHANSE, col. 5, lines 61-63, emphasis added)

Moreover, PHANSE describes the digital filter controller 180 as operating based on analyzing the output of the slicer 155 (which receives the output of the digital FIR filter 150). It is the digital FIR filter 150 that receives the output of the ADC 145.

PHANSE discloses:

"Initially, AEF 140 is set to a preset value (process step 605). For the initial setting of AEF 140, slicer 155 generates a slicer error signal. To reduce or eliminate the slicer error, digital filter controller 180 modifies the filter tap coefficients so that digital FIR filter 160 (sic, should be 150) is adjusted to provide gain sufficient to compensate the channel (process step 610). Based on the converged value of the modified coefficients of digital FIR filter 160, AEF 140 is incremented or decremented so as to partition the optimal balance of gain in the analog and digital data paths for optimal signal-to-noise (SNR) and signal processing requirements (process step 615).

In response to the changes made by AEF 140, slicer 155 generates a new slicer error signal. Again, to reduce or eliminate the slicer error, digital filter controller 180 re-adjusts the filter tap coefficients so that digital FIR filter 160 is adjusted to provide gain sufficient to compensate the channel (process step 620). In response to the new converged value of the modified coefficients of digital FIR filter 160, AEF 140 again is incremented or decremented in order to partition the optimal balance of gain in the analog and digital data paths (process step 625)." (PHANSE, col. 10, line 56 to col. 11, line 10, emphasis added)

According to PHANSE, therefore, for the digital FIR filter 150 to operate at all, the slicer 155 must perform make a hard decision on the output of the digital FIR filter 150, then this hard decision must be provided to the digital filter controller 180, and the digital filter controller 180 then "re-adjusts the filter tap coefficients so that digital FIR filter 160 is adjusted to provide gain sufficient to compensate the channel (process step 620)". This is a feedback type process that is performed using at least 3 separate and distinct functional blocks (i.e., the digital FIR filter 150, the slicer 155, and the digital filter controller 180).

In addition, these very same "filter tap coefficients of digital FIR filter 150 are used to adjust the equalization of AEF 140". In other words, these "filter tap coefficients of digital FIR filter 150" are not only employed to perform modification of the taps of the FIG. filter 150, but they seem necessary to operate to adjust the AEF 140 (i.e., the adaptive equalization filter (AEF) 140 which clearly operates within the "analog domain"). As such, the Applicant respectfully asserts that these Examiner cited portions

of PHANSE teach and disclose a combination analog/digital means of performing equalization before and after the ADC 145 using the adaptive equalization filter (AEF) 140 (that operates on the "analog signal" provided thereto, not "digital samples of the modulated serial data", and whose operation is governed by the "filter tap coefficients of digital FIR filter 150" after having undergone intermediate processing within the analog equalization controller 175.

The Applicant respectfully points out that neither the adaptive equalization filter (AEF) 140 (which operates in the analog domain) nor the digital FIR filter 150 (which operates in the digital domain) is an independently operating device. The adaptive equalization filter (AEF) 140 necessarily operates based on control provided to it from the analog equalization controller 175 (that itself operates based on the filter tap coefficients provided to it from the filter controller 180), and the digital FIR filter 150 also operates based on the filter tap coefficients provided to it from the filter controller 180.

The Applicant in unable to find anywhere in FIG. 1 of PHANSE or the associated description thereof that both of the analog and digital means of equalization are not needed for proper operation. In contradistinction, PHANSE seems only to indicate that the BOTH analog and digital compensation are performed, and only when both are performed, does the compensation for the system of FIG. 1 actually converge.

More specifically, the Applicant respectfully asserts that PHANSE does not teach and disclose a digital signal processed based serializer/de-serializer that adaptively determines compensation to be performed by the receiver on the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein.

In contradistinction, PHANSE teaches and discloses a "mixed mode equalization" approach in many locations such that "analog equalization" as well as "digital equalization" both need to be performed for proper operation. In fact, the Applicant respectfully asserts that the teaching and disclosure of PHANSE is such that the only means by which the "digital equalization" can operate effectively is with the assistance of the "analog equalization". Similarly, the Applicant respectfully asserts that the teaching and disclosure of PHANSE is such that the only means by which the "analog

equalization" can operate effectively is with the assistance of the "digital equalization". Moreover, it appears that the majority of compensation operations are performed in the analog domain, and the digital domain just performs any remaining, fine-tuning compensation when compared to the analog domain compensation.

The Applicant provides some examples from PHANSE that describes this inherent dual analog means in combination with digital means of performing compensation.

"The present invention implements a mixed mode equalization in which analog equalization is performed by adaptive equalization filter 140 and digital equalization is performed by digital FIR filter 150. The mixed mode equalization occurs in alternating digital and analog stages until convergence (or a time out) occurs." (PHANSE, col. 10, lines 5-10, emphasis added)

"FIG. 6 depicts flow diagram 600, which illustrates the mixed mode equalization operation of exemplary full-duplex transceiver 100 according to one embodiment of the present invention. The mixed mode adaptive equalization filter provides signal equalization in the form of a high frequency boost that offsets cable loss. The amount of high frequency boost of the equalizer adapts to the length of the attached cable. Adaptive equalization filter (AEF) 140 is controlled (adapted) in conjunction with digital FIR filter 160. The mixed mode equalization scheme provides some analog and some digital equalization to compensate for the overall attenuation of the channel. AEF 140 is incremented or decremented according to the predetermined converged value of digital FIR filter 160." (PHANSE, col. 10, lines 42-55, emphasis added)

"The above-described mixed mode equalization operation continues in subsequent process steps (such as exemplary process steps 630 and 635) until the coefficients of digital FIR filter 160 converge to the pre-determined threshold value, TH.sub.(AEF). At this point, no further adaptation of AEF 140 is required (process step 640) and the operation is complete." (PHANSE, col. 11, lines 11-17, emphasis added)

Moreover, PHANSE also seems to indicate that the majority of the compensation is performed in the analog domain. For example, when describing another embodiment that deals with the operation of adjusting gain, PHANSE discloses:

"DSP AGC circuit 720 provides additional gain correction entirely in the digital domain. Most gain optimization is performed by AGC circuit 135, but DSP AGC circuit 720 corrects the remainder of the gain and increases the signal for optimum data slicing and detection. Analog AGC circuit 135 maximizes the dynamic range of ADC 145, while keeping the saturation rate below acceptable levels. DSP AGC circuit 720 then boosts the signal to the levels expected by slicer 155. DSP BLW circuit 730 corrects for base line wander, which is an integration effect of the symbol signal through transformer 100 that generates an average or "near DC" base line signal over time. As the base line wanders over time, the slicer decisions of slicer 155 are no longer optimum for the instantaneous data detection. DSP BLW circuit 730 subtracts out the base line signal to keep the effective signal centered at the input of slicer 155.

As noted above, slicer 155 detects the five levels of the PAM-5 signal and generates both an output data signal and an output error signal. The outputs of slicer 155 are used to adapt echo canceller 130 in the analog domain. The outputs of slicer 155 are also used by DSP adaptive controller 740 to control the operations of digital FIR filter 150, DSP echo canceller and NEXT canceller 710, DSP AGC circuit 720, and DSP BLW circuit 730. DSP adaptive controller 740 executes adaptive algorithms that may be updated from time to time by microcontroller-based acquisition state machine 750." (PHANSE, col. 11, lines 60 to col. 12, line 18, emphasis added)

PHANSE teaches and discloses that, in the "digital domain", the "DSP AGC circuit 720 provides additional gain correction". If seems clear that there is also "gain correction" performed exclusively in the analog domain.

The Applicant also respectfully points out that this description of PHANSE cited above is with reference to FIG. 7.

The Applicant respectfully points out that the Examiner does not cite portions of PHANSE when rejecting claim 1, but the Applicant respectfully believes that the description of FIG. 7 of PHANSE, which employs additional digital back-end processing components when compared to FIG. 1, further supports the point that PHANSE does not teach and disclose, or seemingly even to contemplate, the use of digital domain compensation without the assistance of analog domain compensation. As such, the Applicant respectfully believes that one consulting PHANSE would not consider to

modify PHANSE to perform only digital compensation or only analog compensation. Moreover, the Applicant respectfully believes that that one consulting PHANSE would not be led to arrive at the subject matter as claimed by the Applicant in claim 1 of a digital signal processing based serializer/de-serializer. In contradistinction, the Applicant respectfully believes that one consulting PHANSE would be led to arrive at subject matter akin to a device that employs "analog signal processing in combination with digital signal processing".

The Applicant also respectfully believes that the seemingly evident teaching and disclosure of PHANSE that the digital domain based compensation operates in conjunction with the analog domain based compensation (i.e., not independent of it) leads the Applicant to believe that the system of PHANSE would actually be inoperable without the digital domain based compensation operating in conjunction with the analog domain based compensation.

The Applicant respectfully points out that even this FIG. 7 embodiment of PHANSE (which includes much more "digital back-end processing components" than FIG. 1 of PHANSE) requires BOTH analog and digital compensation to operate effectively. One does not even seem capable to operate without the other. The Applicant is unable to find any teaching and disclosure in PHANSE that only one of analog or digital compensation is sufficient for effective operation.

In describing the augmented digital processing capabilities of FIG. 7, PHANSE discloses:

"FIG. 7 illustrates exemplary full-duplex transceiver 700 according to another embodiment of the present invention. In many respects, full-duplex transceiver 700 is identical to full-duplex transceiver 100, particularly in the analog front-end of full-duplex transceiver 700. However, in the digital back-end of full-duplex transceiver 700, new digital signal processing circuitry has been added and existing digital circuitry has been modified." (PHANSE, col. 11, lines 18-25, emphasis added)

Nevertheless, the Applicant respectfully points out that even within this embodiment of FIG. 7 of PHANSE, both the analog and digital compensation needs to be performed for the system to operate effectively. As PHANSE teaches and discloses, the diagram of FIG. 7 depicts almost "identical" in its connectivity between the digital

domain and the analog domain such that at least the analog domain operating components of the DC offset correction controller 160 (which subsequently controls the DC offset correction circuit 125), and the AGC controller 170 (which subsequently controls the automatic gain control (AGC) circuit 135) are governed by the DSP adaptive controller 740 in FIG. 7 of PHANSE.

The Applicant respectfully points out that these compensation operations of PHANSE are performed in the analog domain are not with respect to the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein.

In contradistinction, these compensation operations of PHANSE are performed in the analog domain in conjunction with any operations performed in the digital domain. The Applicant respectfully believes that if the compensation operations of PHANSE were to be performed in the digital domain without the assistance of the compensation operations performed in the analog domain, PHANSE would not operate properly.

Again, PHANSE discloses that "[t]he present invention implements a mixed mode equalization in which analog equalization is performed by adaptive equalization filter 140 and digital equalization is performed by digital FIR filter 150. The mixed mode equalization occurs in alternating digital and analog stages until convergence (or a time out) occurs." (PHANSE, col. 10, lines 5-10, emphasis added)

The Applicant respectfully believes that the system of PHANSE would not "converge" without the combined operation of the "alternating digital and analog stages" that perform analog domain based compensation in conjunction with digital domain based compensation.

The Applicant respectfully points out that PHANSE does not teach and disclose to perform only one of analog based compensation and digital based compensation, but in contradistinction, PHANSE teaches and discloses both analog based compensation and digital based compensation as being complementary and requisite in the proper operation thereof. The effective operation of PHANSE seems inextricably linked to this "mixed mode equalization" that employs both analog based compensation and digital based compensation.

Therefore, in light of at least these comments made above, the Applicant respectfully believes that PHANSE fails to teach and disclose each and every element of the subject matter as claimed by the Applicant in claim 1.

As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claim 1 under 35 U.S.C. § 102(e) as being anticipated by PHANSE.

The Applicant respectfully believes that claims 2-29, being further limitations of the subject matter as claimed in claim 1, are also allowable.

The Applicant respectfully believes that claims 34-41, being further limitations of the subject matter as claimed in claim 1, are also allowable.

With respect to independent claim 42, in the above referenced office action, the Examiner asserts:

"With regard to claim 42, the transceiver claimed is a variation of DSP SERDES of claim 1, and therefore would have been obvious given the aforementioned rejection of claim 1." (office action, Part of Paper No./Mail Date 20050929, p. 8)

The Applicant is unable to find any reference within PHANSE of a plurality of analog to digital converters.

Within FIG. 1 of PHANSE, only one ADC 145 is depicted.

Within FIG. 7 of PHANSE, only one ADC 145 is depicted.

The Applicant is unable to find in PHANSE, and the Applicant respectfully asserts that PHANSE fails to teach and disclose:

a plurality of plurality of analog to digital converters wherein each analog to digital converter within the plurality of analog to digital converters digitally samples analog serial signal to generate digital data arranged across a plurality of channels, each channel of the plurality of channels extends from one analog to digital converter within the plurality of analog to digital converters; and

the digital signal processor adaptively determines a parallel based compensation and a parallel based operation to be performed to ensure a proper characteristic of the digital data.

In light of comments made above as well, in addition to the fact that PHANSE fails to teach and disclose a plurality of analog to digital converters in accordance with the subject matter as claimed by the Applicant in claim 42, the Applicant respectfully

requests that the withdraw the rejection of claim 42 under 35 U.S.C. § 102(e) as being anticipated by PHANSE.

The Examiner also asserts:

"With regard to claims 43-71 and 76-79, these claims are restatements of claims 2-29, and 34-41 and are similarly analyzed." (office action, Part of Paper No./Mail Date 20050929, p. 8)

The Applicant respectfully traverses this assertion of mere restatement with reference to these claims.

The Examiner respectfully believes that claim 42 is allowable in view of at least the comments made above.

The Applicant respectfully believes that claims 43-71 and 76-79, being further limitations of the subject matter as claimed in claim 42, are also allowable.

The Examiner also asserts:

"With regard to claim 11 3, the steps claimed as method are a restatement of the functions of the DSP SERDES of claim 1, and therefore would have been obvious given the aforementioned rejection of claim 1.

With regard to claims 114 - 116 and 119 - 128, these claims are restatements of claims 2 - 29 and 34 - 41, and are similarly analyzed.

With regard to claim 134, Phanse teaches these limitations in claim 1 above, plus the additional of limitation of connection via a trace (see column 3, lines 15 - 25 where this is interpreted as inclusive of backplane).

With regard to claims 135 - 162 and 167 - 174, these claims are restatements of claims 2 - 29 and 34 - 4land are similarly analyzed.

With regard to claim 179, transceiver claimed is a variation of DSP SERDES of claim 1, and therefore would have been obvious given the aforementioned rejection of claim 1.

With regard to claim 180, Phanse teaches these limitations in claim 179 above, plus the additional of limitation of connection via a trace (see column 3, lines 15 - 25 where this is interpreted as inclusive of backplane)." (office action, Part of Paper No./Mail Date 20050929, p. 8-9)

The Applicant respectfully traverses this assertion of mere restatement with reference to these claims.

Therefore, the Applicant respectfully asserts that PHANSE fails to teach and disclose each and every element of the subject matter as claimed by the Applicant in claims 1-29, 34-71, 76-79, 113-116, 119-128, 134-162, 167-174, 179, and 180.

In light of at least these comments, the Applicant respectfully believes that claims 1-29, 34-71, 76-79, 113-116, 119-128, 134-162, 167-174, 179, and 180 are allowable over PHANSE.

As such, the Applicant respectfully requests that the Examiner withdraw the rejections to claims 1-29, 34-71, 76-79, 113-116, 119-128, 134-162, 167-174, 179, and 180 under 35 U.S.C. § 102(e) as being anticipated by PHANSE.

Claim Rejections - 35 U.S.C. § 103

3. In the office action, the Examiner states:

"Claims 30 - 33, 72 - 75, 80 - 112, 117, 118, and 163 - 166 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phanse('494) in view of Jamali (US-6,678,319)." (Jamali (US-6,678,319) is hereinafter referred to as "JAMALI") (office action, Part of Paper No./Mail Date 20050929, p. 9).

The Applicant respectfully traverses.

The Applicant's comments made above with respect to the Examiner's 35 U.S.C. § 102 rejection based on PHANSE are also applicable here.

The Applicant respectfully believes that JAMALI fails to overcome the deficiencies of PHANSE with respect to independent claims 1, 42, 113, and 134.

With respect to independent claim 80, the Examiner asserts:

"With regard to claim 80, Phanse discloses the limitations of a transceiver as analyzed in claim 1 but is silent with respect to feedback equalizer. Jamali discloses a transceiver utilizing a feedback equalizer (see figure 5, 528) for adjustment of channel characteristics (see column 5, lines 19 - 51). It would have been obvious to one of ordinary skill in the art at the time of invention to utilize a feedback equalizer to improve system performance (see '319, column 3, lines 48 - 51)." (office action, Part of Paper No./Mail Date 20050929, p. 10)

The Applicant respectfully believes that JAMALI fails to overcome the deficiencies of PHANSE with respect to independent claim 80.

In view of at least the Applicant's comments made above, the Applicant respectfully believes that PHANSE fails to teach and disclose the subject matter of independent claim 80 that includes at least a transceiver, comprising: a receiver comprising a plurality of analog to digital converters and a digital signal processor; and wherein each analog to digital converter within the plurality of analog to digital converters sequentially samples analog serial signal to generate digital data arranged across a plurality of channels; each channel of the plurality of channels extends from one analog to digital converter within the plurality of analog to digital converters; the digital signal processor comprises at least one of a feedback equalizer and a decision feedback equalizer that is operable to adaptively identify error information that is used to determine a parallel based compensation and a parallel based operation to be performed to ensure a proper characteristic of the digital data; the parallel based operation comprises adjusting an operational parameter of at least one analog to digital converter within the plurality of analog to digital converters; and the digital signal processor communicates feedback control individually to each analog to digital converter within the plurality of analog to digital converters.

As mentioned above, the Applicant is unable to find a plurality of analog to digital converters in PHANSE.

Even assuming the accuracy of the Examiner's assertion that "Jamali discloses a transceiver utilizing a feedback equalizer (see figure 5, 528) for adjustment of channel characteristics (see column 5, lines 19 - 51)", the Applicant respectfully points out that one would not arrive at the subject matter as claimed by the Applicant in claim 80 by combining JAMALI with PHANSE.

As such, the Applicant respectfully believes that claim 80 is patentable over PHANSE in view of JAMALI.

The Applicant respectfully believes that claims 30-33, being further limitations of the subject matter as claimed in claim 1, either directly or interveningly, are also allowable.

The Applicant respectfully believes that claims 72-75, being further limitations of the subject matter as claimed in claim 42, either directly or interveningly, are also allowable.

The Applicant respectfully believes that claims 81-112, being further limitations of the subject matter as claimed in claim 80, either directly or interveningly, are also allowable.

The Applicant respectfully believes that claims 117, 118, being further limitations of the subject matter as claimed in claim 113, either directly or interveningly, are also allowable.

The Applicant respectfully believes that claims 163, 166, being further limitations of the subject matter as claimed in claim 134, either directly or interveningly, are also allowable.

In view of at least these comments as well as the comments made above, the Applicant respectfully believes that claims 30 - 33, 72 - 75, 80 - 112, 117, 118, and 163 - 166 are allowable over PHANSE in view of JAMALI.

As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 30 - 33, 72 - 75, 80 - 112, 117, 118, and 163 - 166 under 35 U.S.C. § 103(a) as being unpatentable over PHANSE in view of JAMALI.

4. In the office action, the Examiner states:

"Claims 129 - 133, 175 - 178, and 181 - 184 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phanse ('494) in view of Apple (US-5,239,299)." (Apple (US-5,239,299)" is hereinafter referred to as "APPLE") (office action, Part of Paper No./Mail Date 20050929, p. 11).

The Applicant respectfully traverses.

In claim 129, the Applicant claims subject matter including at least a method to perform digital signal processing based de-serialization of analog serial signal, the method comprising: pre-computing a plurality of possible compensation operation options; receiving analog serial signal; digitally, sequentially sampling the analog serial signal to generate digital data using a plurality of interleaved analog to digital converters; analyzing the digital data, using a digital signal processor, to adaptively determine

whether any compensation is required to ensure a proper characteristic of the digital data by employing digital signal processing techniques; selecting a compensation operation when it is determined that compensation is required, the compensation operation being selected to ensure the proper characteristic, the compensation operation being selected from the plurality of possible compensation operation options; providing compensation control to a device that is operable to perform the compensation operation; and wherein the compensation, when required, is implemented by adjusting an operational characteristic of at least one analog to digital converter within the plurality of interleaved analog to digital converters.

The Applicant in unable to find in PHANSE that the any operational characteristic of the ADC 145 is even capable of being adjusted.

PHANSE teaches and discloses that the signal input to or output from the ADC 145 can be modified, but the ADC 145 itself does not appear to be undergoing any adjustment of an operational parameter therein.

For example, PHANSE discloses:

"However, in some embodiments, the signal levels of the output of ADC 145 may not match the signal levels expected by slicer 155. That is, it may not be possible to operate ADC 145 to reach the signal levels suitable for slicer 155 without sacrificing the extra headroom needed to prevent saturation of ADC 145. To compensate for this, in an advantageous embodiment of the present invention, digital FIR filter 150 may also apply a flat gain to the digital output of ADC 145 in addition to applying signal equalization to the output of ADC 145. The gain applied by digital FIR filter 150 may scale up or scale down the digital output signals from ADC 145." (PHANSE, col. 6, line 63 to col. 7, line 7, emphasis added)

The ADC 145 appears to be a dumb device that with respect to this gain functionality described herein, given that it is prone to "saturation" and gain of signals must be adjusted either before being put into the ADC 145 or output from the ADC 145.

Moreover, the only input being provided to the ADC is from the clock recovery mixer 190 within FIG. 1 and FIG. 7.

PHANSE discloses:

"Full duplex transceiver 100 also comprises timing recovery control circuit 185 and clock recovery mixer 190, which generates a recovered clock signal from the outputs of slicer 155. Timing recovery control circuit 185 and clock recovery mixer 190 use the data signal and error signal from slicer 155 as inputs to a digital phase-locked loop (PLL) circuit. The PLL circuit controls the phase/delay of an analog-based frequency synthesizer which, in turn, produces a low jitter clock centered at the symbol for sampling by ADC 145." (PHANSE, col. 5, line 66 to col. 6, line 5, emphasis added)

The Applicant respectfully points out that "clock recovery mixer 190", which provides the input signal to the ADC 145 from the top in FIG. 1 and FIG. 7 of PHANSE, is only mentioned twice in all of PHANSE, and these two occurrences are in the cited portion above.

In PHANSE, the Applicant respectfully points out that the signal provided to the ADC 145 from the clock recovery mixer 190 is a "low jitter clock".

The Applicant respectfully points out that the providing of a clock to a device does not typically perform any adjusting an operational characteristic of the device. PHANSE is silent as to whether the "low jitter clock" provided to the ADC 145 from the clock recovery mixer 190 performs any adjustment of an operational parameter therein.

In view of at least these comments as well as the comments made above, the Applicant respectfully believes that claims 129 - 133, 175 - 178, and 181 - 184 are allowable over PHANSE and further in view of APPLE.

As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 129 - 133, 175 - 178, and 181 - 184 under 35 U.S.C. § 103(a) as being unpatentable over PHANSE in view of APPLE.

The Applicant respectfully believes that claims 1-184 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present patent application.

RESPECTFULLY SUBMITTED,

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